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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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INTEL CORPORATION c/o INTELLEVATE, LLC P.O. BOX 52050 MINNEAPOLIS, MN 55402			EXAMINER CHOE, YONG J	
			ART UNIT 2185	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/629,093

Applicant(s)

ROYER, ROBERT J.

Examiner

Yong Choe

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 June 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

1. The examiner acknowledges the applicant's submission of the amendment filed on 06/22/2007. At this point, claims 13-21 and 25-27 have been amended. Thus, claims 1-27 are pending in the instant application.
2. The objection to the drawing has been withdrawn as necessitated by amendment.
3. The objection to claims 13-21 and 25-27 has been withdrawn as necessitated by amendment.
4. The rejection under 35 USC § 101 to claims 13-21 and 25-27 has been withdrawn as necessitated by amendment.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 1, 5, 6, 13, 17, 18, 22-24 and 25-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Liao et al. (US Publication No.: US 2002/0062424)** in view of **Thelin et al. (US Patent No.: US 6,961,814)**.

Regarding independent claims 1, 13, 22 and 25, Liao et al. discloses a method in a Constant Access Time Bounded (CATB) cache, comprising:

reserving a first number of unallocated lines in the cache for pinned data (i.e., locked cache), the first number being less than the number of lines in the cache; and if data needs to be inserted into the cache as pinned data (i.e., locked cache) ([0018] and [0022]).

Liao et al. further teaches initializing a search group of the CATB cache with a capability to dynamically insert and delete elements ([0020]).

However, Liao et al. does not specifically teach selecting a line from the lines reserved for pinned data; storing the data in the line; and inserting the line into a search group of the CATB cache.

Thelin et al. teaches selecting a line from the lines reserved for pinned data (Fig. 2B: Free Links); storing the data in the line; and inserting the line into a search group of the CATB cache (Fig.8 and col.6, lines 17-29: updating linked lists reads on this limitation).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate selecting a replacement line from a reserve of cache lines and inserting the replacement line into the search group as taught by Thelin et al. into the management of on-chip cache of Liao et al. in order to expedite the allocation process for a host command (col.1, lines 42-43).

Therefore, it would have been obvious to combine selecting a replacement line from a reserve of cache lines and inserting the replacement line into the search group

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as taught by Thelin et al. with the management of on-chip cache of Liao et al. to obtain the invention.

Regarding claims 5 and 17, Liao et al. teaches wherein inserting the line into a search group of the cache further comprises: indicating that the line is allocated; indicating that the line is pinned; and using a tag of the line to map the line to a search group of the cache ([0020]).

Regarding claims 6 and 18, Liao teaches the CATB cache is implemented as a set-associative cache; each search group of the cache is a set of the cache; and inserting the line into a search group of the cache further comprises: using the address of the data as the tag of the line; performing a modulus operation between the tag and the number of sets (N) in the cache (the tag MOD N) to map the tag to a set of the cache; performing a search based on the tag of the line; and inserting the line into a dynamic data structure that represents the set ([0035]).

Regarding claims 23 and 26, Thelin et al. teaches receiving a first identifier for an element; using the first identifier to compute a second identifier for a search group in the CATB cache; and traversing the search group to locate an element matching the first identifier (col.2, lines 14-35).

Regarding claims 24 and 27, Thelin et al. teaches wherein the search group is implemented as a linked list (col.1, lines 64-67 and col.2, lines 1-3).

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7. **Claims 2 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Liao et al. (US Publication No.: US 2002/0062424)** in view of **Thelin et al. (US Patent No.: US 6,961,814)** and in further view of **Norman (US Patent No.: US 6,292,868)**.

Regarding claims 2 and 14, Liao et al. and Rowlands do not specifically teach wherein each line of the cache is stored in non-volatile memory.

However, Norman teaches wherein each line of the cache is stored in non-volatile memory (col.6, lines 15-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate each line of the cache is stored in non-volatile memory as taught by Norman into the management of on-chip cache of Liao et al. as modified by Thelin et al. in order to increase speed and reliability (col.6, lines 14-16).

Therefore, it would have been obvious to combine each line of the cache is stored in non-volatile memory as taught by Norman with the management of on-chip cache of Liao et al. as modified by Thelin et al. to obtain the invention.

8. **Claims 3, 4, 15 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Liao et al. (US Publication No.: US 2002/0062424)** in view of **Thelin et al. (US Patent No.: US 6,961,814)** and in further view of **Norman (US Patent No.: US 6,292,868)** and **Wong (US Patent No.: US 7,130,979)**.

Regarding claims 3 and 15, Wong Liao et al., Thelin et al. and Norman do not specifically teach recovering the organization of the cache on power up following a loss of power to the cache by in a first phase of recovery, for each line in the cache determining if the line is allocated; if the line is allocated, inserting the line in a search group of the cache; and if the line is not allocated, inserting the line into a pool of free lines; and in a second phase of recovery, for each search group determining the number of pinned lines in the search group; and adding at least one line from the pool of free lines to each search group that has at least one pinned line.

However, Wong teaches recovering the organization of the cache on power up following a loss of power to the cache by in a first phase of recovery, for each line in the cache determining if the line is allocated; if the line is allocated, inserting the line in a search group of the cache; and if the line is not allocated, inserting the line into a pool of free lines; and in a second phase of recovery, for each search group determining the number of pinned lines in the search group; and adding at least one line from the pool of free lines to each search group that has at least one pinned line (Fig.9, col.9, lines 50-67 and col.10, lines 1-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate recovering system as taught by Wong into the management of on-chip cache of Liao et al. as modified by Thelin et al. and Norman in order to ensure that valid volume definition is available even in the event of a power loss (col.4, lines 47-48).

Therefore, it would have been obvious to combine recovering system as taught by Wong with the management of on-chip cache of Liao et al. as modified by Thelin et al. and Norman to obtain the invention.

Regarding claims 4 and 16, Wong teaches wherein the cache is a disk cache in a processor based system (col.1, lines 55-58).

9. **Claims 7 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Liao et al. (US Publication No.: US 2002/0062424)** in view of **Thelin et al. (US Patent No.: US 6,961,814)** and in further view of **Mandal et al. (US Patent No.: US 6,983,465)**.

Regarding claims 7 and 19, Liao et al. and Thelin et al. do not specifically teach wherein indicating that the line is pinned further comprises modifying metadata associated with the line to indicate that the line is pinned.

However, Mandal et al. teaches wherein indicating that the line is pinned further comprises modifying metadata associated with the line to indicate that the line is pinned (Fig.8 and col.13, lines 36-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate managing data caching of Mandal et al. into the management of on-chip cache of Liao et al. as modified by Thelin et al. in order to view and control the system (col.2, line 29).

Therefore, it would have been obvious to combine managing data caching of Mandal et al. with the management of on-chip cache of Liao et al. as modified by Thelin et al. to obtain the invention.

10. **Claims 8, 10, 12 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Liao et al. (US Publication No.: US 2002/0062424)** in view of **Rowlands (US Patent No.: US 6,748,492)**.

Regarding independent claims 8, 10, 12 and 20, Liao et al. discloses for a whole number N, in an N-way set associative non-volatile disk cache, a method comprising:

reserving a predetermined number of lines for pinned data and organizing them into a pool of lines for pinned data ([0018]); distributing the remaining lines in the cache into N dynamic data structures of approximately the same size to represent the N sets of the cache ([0020]);

Liao et al. does not specifically teach if data is to be inserted into the cache as pinned data, inserting the data into a line from the pool for pinned data; marking the line as allocated by modifying metadata associated with the line; determining the set to which the line belongs using a mapping based on the tag associated with the line; removing the line from the pool for pinned data; and adding the line to the set.

However, Rowlands teaches if data is to be inserted into the cache as pinned data, inserting the data into a line from the pool for pinned data; marking the line as

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allocated by modifying metadata associated with the line (col.9, lines 42-53); determining the set to which the line belongs using a mapping based on the tag associated with the line; removing the line from the pool for pinned data; and adding the line to the set (col.9, lines 47-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the N way set associative as taught by Rowlands into the management of on-chip cache of Liao et al. in order to ensure that a particular entry is used for a particular transaction (col.1, lines 65-66).

Therefore, it would have been obvious to combine incorporate the N way set associative as taught by Rowlands with the management of on-chip cache of Liao et al. to obtain the invention.

11. **Claims 9, 11 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Liao et al. (US Publication No.: US 2002/0062424)** in view of **Rowlands (US Patent No.: US 6,748,492)** and in further view of **Wong (US Patent No.: US 7,130,979)**.

Regarding claims 9, 11 and 21, Liao et al. and Rowlands do not specifically teach recovering the organization of the cache on power up following a loss of power to the cache by in a first phase of recovery, for each line in the cache determining if the line is allocated; if the line is allocated, inserting the line in a set of the cache using a mapping based on the tag associated with the line; and if the line is not allocated,

inserting the line into a pool of unallocated lines; and in a second phase of recovery, for each set in the cache determining the number of pinned lines in the set using the metadata associated with each line in the set; and moving one or more lines from the pool of unallocated lines to each set that has at least one pinned line so that the number of non-pinned lines in each set is approximately the same.

However, Wong teaches recovering the organization of the cache on power up following a loss of power to the cache by in a first phase of recovery, for each line in the cache determining if the line is allocated; if the line is allocated, inserting the line in a set of the cache using a mapping based on the tag associated with the line; and if the line is not allocated, inserting the line into a pool of unallocated lines; and in a second phase of recovery, for each set in the cache determining the number of pinned lines in the set using the metadata associated with each line in the set; and moving one or more lines from the pool of unallocated lines to each set that has at least one pinned line so that the number of non-pinned lines in each set is approximately the same (Fig.9, col.9, lines 50-67 and col.10, lines 1-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate recovering system as taught by Wong into the management of on-chip cache of Liao et al. as modified by Rowlands in order to ensure that valid volume definition is available even in the event of a power loss (col.4, lines 47-48).

Therefore, it would have been obvious to combine recovering system as taught by Wong with the management of on-chip cache of Liao et al. as modified by Rowlands

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to obtain the invention.

Citations of Relevant Art

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takahashi et al. (US Patent No.: US 6,434,666) discloses memory control apparatus and method for storing data in a selected cache memory based on whether a group or slot number is odd or even.

Response to Arguments

13. Applicant's arguments filed on 06/22/2007 have been fully considered but they are not persuasive.

1st Point of Argument

Regarding Applicant's remarks on pages 14,15 and 17, the applicants argue that Liao does not disclose "a portion of the cache is reserved for cache lines that are retained potentially indefinitely in the cache and are not subject to the normal cache replacement policy, that is, reserving a portion of a cache for pinned data".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a cache line that is retained potentially indefinitely in the cache and are not subject to the normal cache replacement policy is said to be "pinned.") are not recited

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in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

While this is unlike applicant's disclosed claimed device, this reads on broad claimed language.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

15. Any inquiry concerning this communication should be directed to **Yong Choe** at telephone number **571-270-1053**. The examiner can normally be reached on M-F 8:00am to 5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Sanjiv Shah** can be reached on **571-272-4098**. Any inquiry

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of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-irect.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER



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